

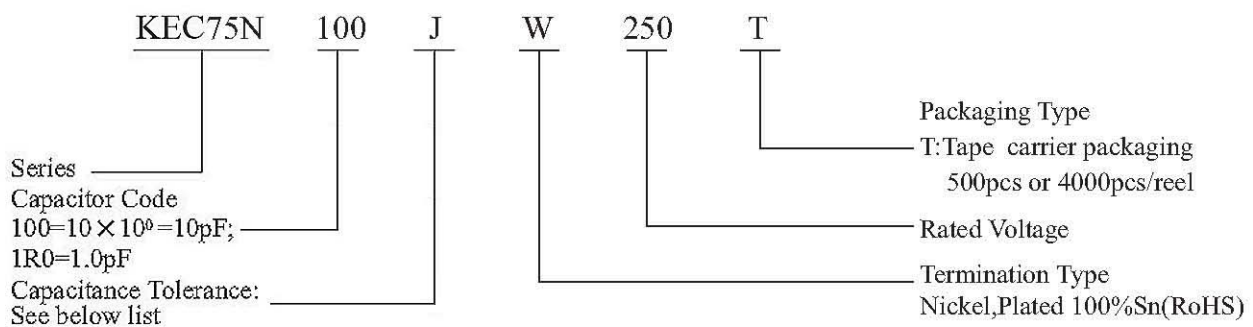
**KEC75N(0201)**

◆ **KEC75N Capacitance Table**

Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC
0.1	0R1	A,B, C,D	25V Code 250 or 50V Code 500	2.2	2R2	A,B, C,D	25V Code 250 or 50V Code 500	16	160	E,G, J	25V Code 250 or 50V Code 500
0.2	0R2			2.4	2R4			18	180		
0.3	0R3			2.7	2R7			20	200		
0.4	0R4			3.0	3R0			22	220		
0.5	0R5			3.3	3R3			24	240		
0.6	0R6			3.6	3R6			27	270		
0.7	0R7			3.9	3R9			30	300		
0.8	0R8			4.3	4R3			33	330		
0.9	0R9			4.7	4R7			36	360		
1.0	1R0			5.1	5R1			39	390		
1.1	1R1			5.6	5R6			43	430		
1.2	1R2			6.2	6R2			47	470		
1.3	1R3			6.8	6R8			51	510		
1.4	1R4			7.5	7R5			56	560		
1.5	1R5			8.2	8R2			62	620		
1.6	1R6			9.1	9R1	68	680				
1.7	1R7			10	100	75	750				
1.8	1R8			11	110	82	820				
1.9	1R9			12	120	91	910				
2.0	2R0			13	130	100	101				
2.1	2R1			15	150						

Remark: special capacitance, tolerance and WVDC are available, consult with Kete.


◆ **Part Numbering**



Code	A	B	C	D	F	G	J
Tolerance	± 0.05pF	± 0.1pF	± 0.25pF	± 0.5pF	± 1%	± 2%	± 5%

### ◆ KEC75N Chip Dimensions

unit: inch(millimeter)

Series	Term. Code	Type / Outlines	Capacitor Dimensions				Plated Material
			Length (L <sub>c</sub> )	Width (W <sub>c</sub> )	Thickness (T <sub>c</sub> )	Overlap (B)	
KEC75N	W	 Chip	.024 ± .001 (0.60 ± 0.03)	.012 ± .001 (0.30 ± 0.03)	.012 ± .001 (0.30 ± 0.03)	.008 (0.20) max	Sn/Ni (RoHS)

### ◆ Design Kits

These capacitors are 100% RoHS. Kits contain 10(ten) pieces per value; number of values per kit varies, depending on case size and capacitance.

Kit	Description (pF)	Values (pF)	Tolerance
DKKEC75N01	0.1 - 2.0	0.1, 0.2, 0.3, 0.5, 0.7, 0.8, 0.9, 1.0, 1.3, 1.5, 1.7, 1.9, 2.0	± 0.10pF
DKKEC75N02	1.0 - 10	1.0, 1.3, 1.5, 1.7, 1.9, 2.0, 2.2, 2.7, 3.0, 3.9, 4.7, 5.6, 6.8, 7.5, 8.2	± 0.10pF
		10	± 5%
DKKEC75N03	10 - 33	10, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33	± 5%

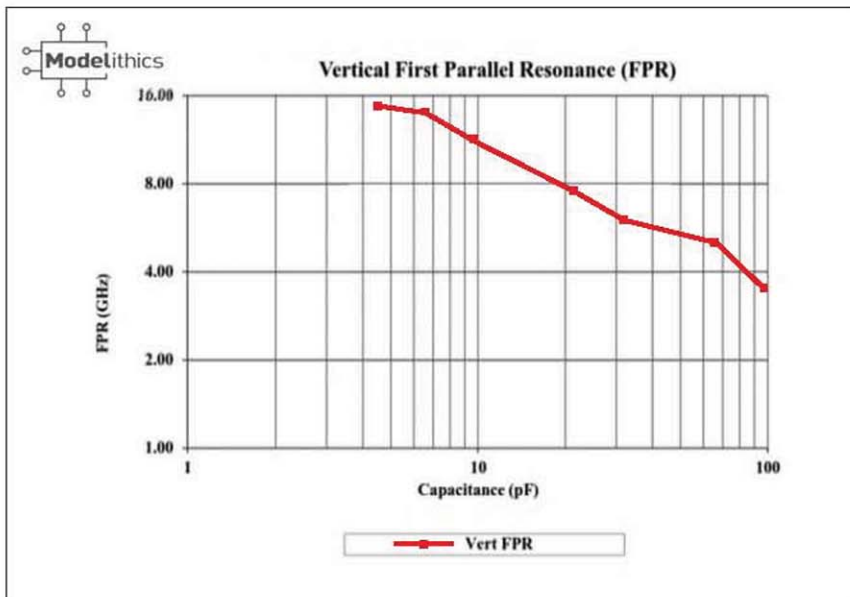
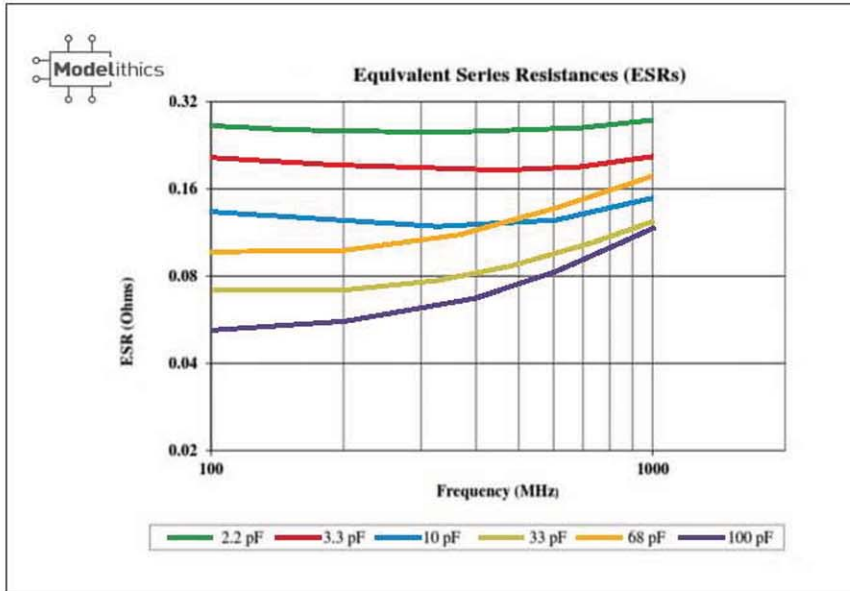
### ◆ Performance

Item	Specifications
Quality Factor (Q)	2,000 min.
Insulation Resistance (IR)	10 <sup>5</sup> Megohms min. @ +25 °C at rated WVDC. 10 <sup>4</sup> Megohms min. @ +125 °C at rated WVDC.
Rated Voltage	25V
Dielectric Withstanding Voltage (DWV)	250% of rated voltage for 5 seconds.
Operating Temperature Range	-55 °C to +175 °C
Temperature Coefficient (TC)	0 ± 30ppm/°C
Capacitance Drift	± 0.02% or ± 0.02pF, whichever is greater.
Piezoelectric Effects	None

**◆ Environmental Tests**

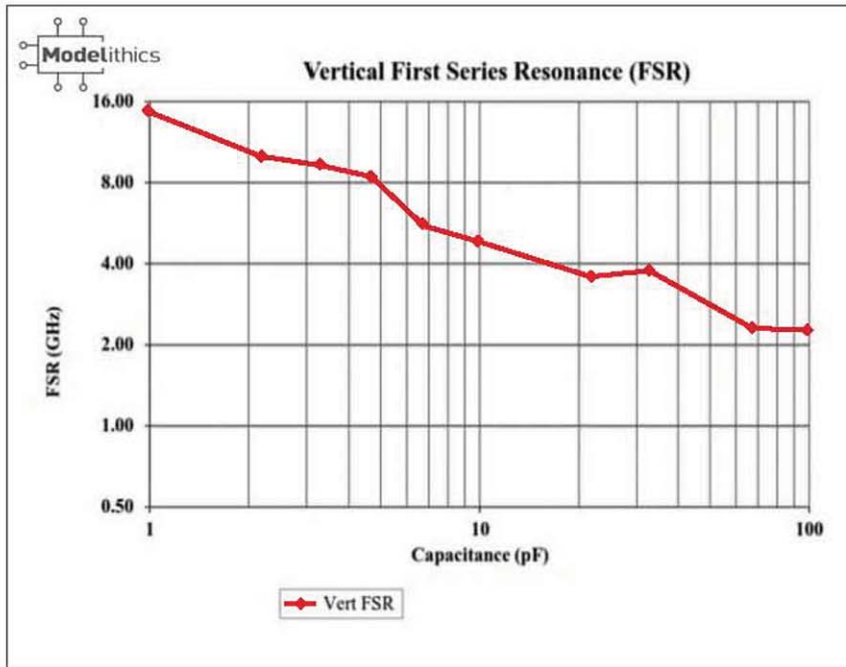
Item	Specifications	Method
Terminal Adhesion	Termination should not pull off. Ceramic should remain undamaged.	Linear pull force exerted on axial leads soldered to each terminal. 2.0lbs.
Resistance to soldering heat	No mechanical damage Capacitance change: $-1.0\% \sim +2.0\%$ $Q > 500$ I.R. $> 10 \text{ G Ohms}$ Breakdown voltage: $2.5 \times \text{WVDC}$	Preheat device to $150^{\circ}\text{C}$ - $180^{\circ}\text{C}$ for 60 sec. Dip in $260^{\circ}\pm 5^{\circ}\text{C}$ solder for $10\pm 1$ sec. Measure after $24\pm 2$ hours cooling period.
Thermal Shock	No mechanical damage Capacitance change: $\pm 0.5\%$ or $0.5\text{pF max}$ $Q > 2000$ I.R. $> 10 \text{ G Ohms}$ Breakdown voltage: $2.5 \times \text{WVDC}$	MIL-STD-202, Method 107, Condition A. At the maximum rated temperature ( $-55^{\circ}\text{C}$ and $125^{\circ}\text{C}$ ) stay 30 minutes. The time of removing shall not be more than 3 minutes. Perform the five cycles.
Humidity, Steady State	No mechanical damage Capacitance change: $\pm 0.5\%$ or $0.5\text{pF max}$ . $Q > 300$ I.R. $> 1 \text{ G Ohms}$ Breakdown voltage: $2.5 \times \text{WVDC}$	MIL-STD-202, Method 106.
Low Voltage Humidity	No mechanical damage Capacitance change: $\pm 0.3\%$ or $0.3\text{pF max}$ . $Q > 300$ I.R. $> 1 \text{ G Ohms}$ Breakdown voltage: $2.5 \times \text{WVDC}$	MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of $85^{\circ}\text{C}$ with 85% relative humidity for 240 hours minimum.
Life	No mechanical damage Capacitance change: $\pm 2.0\%$ or $0.5\text{pF max}$ . $Q > 500$ I.R. $> 1 \text{ G Ohms}$ Breakdown voltage: $2.5 \times \text{WVDC}$	MIL-STD-202, Method 108, for 1000 hours, at $125^{\circ}\text{C}$ . 200% Rated voltage D.C. applied.

◆ **KEC75N Performance Curve**



The First Parallel Resonance, FPR, is defined as the lowest frequency at which a suckout or notch appears in |S21|. It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A horizontal orientation means the electrode planes are parallel to the substrate.

◆ **KEC75N Performance Curve**



The First Series Resonance, FSR, is defined as the lowest frequency at which the imaginary part of the input impedance,  $\text{Im}[Z_{in}]$ , equals zero. Should  $\text{Im}[Z_{in}]$  or the real part of the input impedance,  $\text{Re}[Z_{in}]$ , not be monotonic with frequency at frequencies lower than those at which  $\text{Im}[Z_{in}] = 0$ , the FSR shall be considered as undefined. FSR is dependent on internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined alongside the FPR plot; and mounting pad dimensions.

**Definitions and Measurement Conditions:**

The definitions on the FPR and FSR charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with a 50-Ohm termination. The measurement conditions are: substrate -- Rogers RO3006; substrate dielectric constant -- 6.15; substrate thickness (mils) -- 10; gap in microstrip trace (mils) -- 6.0; microstrip trace width (mils) -- 14.1; Reference planes at sample edges.

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by Kete. The models are derived from measurements on a large number of parts disposed on several different substrates.